6.012 Design Project 1

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Contents

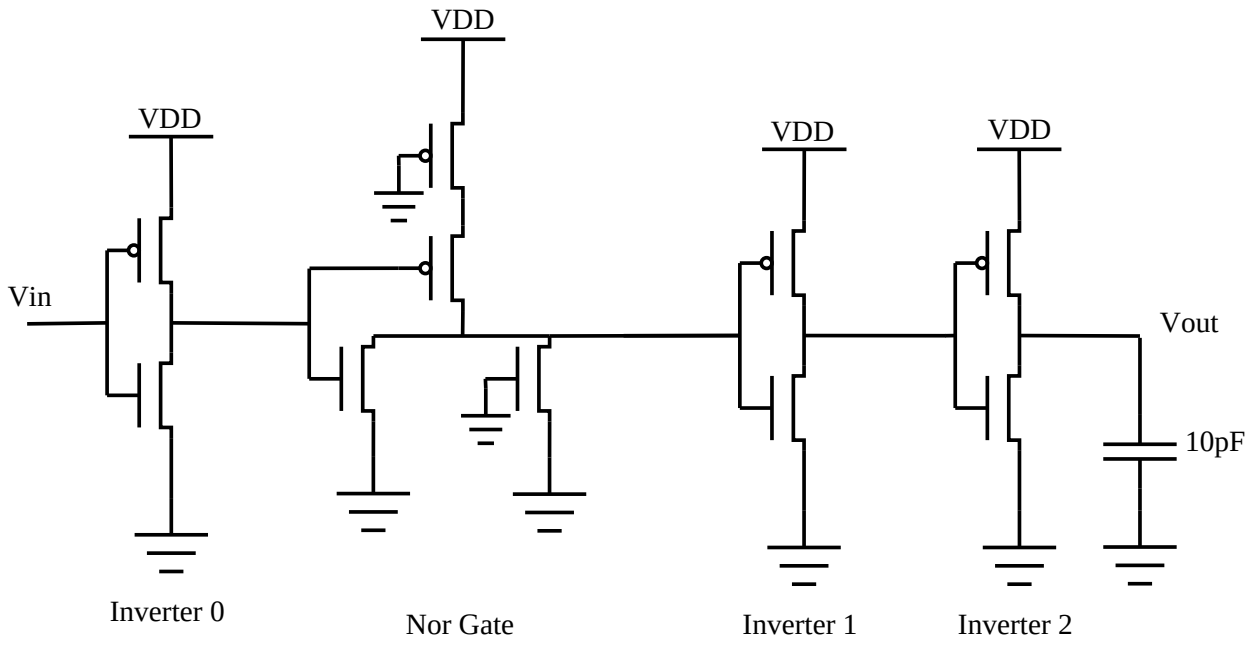

Figure 1: System Schematic

1 Introduction

In order to build this driver, we need to specify the number of inverters used, the width and length of all transistors, and the final inverter's supply voltage V_{DDIO}. Calculating device lengths is simple since all lengths are fixed at $L = 1.5\mu$.

Because the driver is supposed to maintain a $V_M = V_{DD}/2$, we can assume as a first approximation that the width of the p-device is twice that of the corresponding n-device for all inverters. This is because

$$V_M = \frac{V_{Tn} + (V_{DD} + V_{Tp})\sqrt{\frac{k_n}{k_p}}}{1 + \sqrt{\frac{k_n}{k_p}}}$$

Setting $V_M = V_{DD}/2$, we obtain $k_p/k_n = 1$. However, since $k_n = \frac{W_n}{L}\mu_n C_{ox}$ and $k_p = \frac{W_p}{L}\mu_p C_{ox}$, we can determine that

$$\frac{k_n}{k_p} = 1 = \frac{W_n\mu_n}{W_p\mu_p} = \frac{2\mu_p W_n}{\mu_p W_p} = \frac{2W_n}{W_p}$$

which leads us to conclude that $W_n = 2W_p$.

Later on we will tweak this assumption. Sizing of the NOR gate is similar. In the worst case, each p-device must supply enough current to satisfy both n-devices. This suggests that $W_p = 4W_n$ for the NOR gate. However, because the second p-device has it's back tied to V_{DD} while it's source is not at V_{DD}, this device will see a nonzero source to back voltage V_{SB}. Consequently, this device will exhibit a larger threshold than expected. Since the back gate effect is difficult to calculate, we will need to tweak the NOR gate's p to n width ratio using hspice to set V_M properly.

Now that we have some constraints, we need to find the widths of the n-devices and the supply voltage V_{DDIO}. We know that the propagation delay and power consumption of an individual gate

are approximated by:

$$t_{PD} = \frac{(C_{DB} + C_L) V_{DD} L}{2W_n \mu_n C_{ox} (V_{DD} - V_{Tn})^2} + \frac{(C_{DB} + C_L) V_{DD} L}{2W_p \mu_p C_{ox} (V_{DD} + V_{Tp})^2}$$

$$P = f V_{DD}^2 (C_{DB} + C_L)$$

Note that C_{DB} is the parasitic drain-to-bulk capacitance and is approximated by

$$C_{DB} = L_{diff} w_n C_{jn} + L_{diff} w_p C_{jp} + (w_n + 2L_{diff}) C_{jswn} + (w_p + 2L_{diff}) C_{jswp}$$

while C_L is the load capacitance seen by that particular gate. For the last gate, this load capacitance is 10pF. For the other gates, this load capacitance equals the total input capacitance of the following gate: $C_{IN} = C_{ox} L (w_n + w_p)$. The total delay for the circuit is then $t_{PD} = t_{PD,NOR} + t_{PD1} + t_{PD2}$ while the total power consumed is approximated by

$$P = f V_{DD} (C_{G,NOR} + C_{DB,NOR} + C_{G1} + C_{DB1} + C_{G2}) + f V_{DDIO}^2 (C_{DB2} + C_L)$$

To simplify the math, we will assume that $w_{n+1} = a w_n$ where a is a factor to be determined. Since the first inverter has an n-device width of 6μ, $w_n = 6a$ for the NOR gate and $w_n = 6a^2$ for inverter 1. However, finding the optimal device width for the last inverter is tricky due to power and delay tradeoffs involving V_{DDIO}, so we will leave that as a variable to optimize for. We will start by assuming that $V_{DDIO} = 2V$ initially. Combining these constraints, we arrive at the following formulas for total propagation delay and power consumption:

$$t_{PD} = 0.31 + \frac{0.018}{a} + 0.11a + \frac{0.02 + 0.02 w_{n2}}{a^2} + \frac{264}{w_{n2}}$$

$$P = 2.01 + 0.073a + 0.043a^2 + 0.0057 w_{n2}$$

To solve for t_{PD} and P, we first minimize t_{PD} as a function of w_{n2}. This yields a relation between w_{n2} and a. We then substitute this relation into our expression for power consumption reducing it to a function of a only. Finally, we set our simplified power expression equal to our target power, and solve this for a. This allows us to determine w_{n2}. This is how we proceed:

$$\frac{dt_{PD}}{dw_{n2}} = 0 \rightarrow \frac{0.02}{a^2} - \frac{264}{w_{n2}^2} = 0 \rightarrow w_{n2} = 114a$$

$$P|_{w_{n2}=114a} = 2.01 + 0.72a + 0.043a^2 - 3.5 = 0 \rightarrow a = 1.9 \rightarrow w_{n2} = 210\mu$$

These hand calculations suggest that $V_{DDIO} = 2V$ and that the gates' n-devices have the following widths: 12μ, 24μ, 200μ while the p-devices have these widths: 48μ, 48μ, 400μ. After starting with these assumptions, careful iterated analysis with hspice yielded the device parameters described in Table 1. These parameters differ in several ways from the original set derived from the hand calculations. For one thing, the ratio of p-device to n-device width for NOR gate has decreased in order to compensate for the threshold problems caused by the backgate effect. In addition, the NOR gate's n-device is approximately 4 times the size of the n-device in inverter 0. This change was made to improve speed. Because the target delay time is measured as the delay between the NOR gate and the output, slowing down inverter 0 does not affect the total propagation delay much. That means that increasing the NOR gate's size relative to the size of inverter 0 improves the NOR gate's delay at the cost of inverter 0's delay (which does not count toward the total delay specification).

Other changes include slightly increasing Inverter 2's n-device width in order to reduce delay and slightly decreasing inverter 1's p-device width in order to reduce power consumption.

Gate	Transistor	Width	Supply Voltage	Area
Inverter 0	p	12μ	V_{DD}	162 μ^2
Inverter 0	n	6μ	V_{DD}	81 μ^2
NOR	p (top)	74μ	V_{DD}	999 μ^2
NOR	p (bottom)	74μ	V_{DD}	999 μ^2
NOR	n (left)	24μ	V_{DD}	324 μ^2
NOR	n (right)	24μ	V_{DD}	324 μ^2
Inverter 1	p	135μ	V_{DD}	1823 μ^2
Inverter 1	n	90μ	V_{DD}	1215 μ^2
Inverter 2	p	408μ	V_{DDIO}	5508 μ^2
Inverter 2	n	204μ	V_{DDIO}	2754 μ^2

The total area is $12,865\mu^2$.

2 Hand calculations

2.1 NOR Gate

Since the NOR gate has two n-devices of width 24 and two p-devices of width 74, it's total area should be $A_{NOR} = 2(w_n + w_p)(L + 2L_{diff}) = 2646\mu^2$. The NOR gate is driving Inverter 1, so it's gate capacitance is equal to Inverter 1's input capacitance, $C_{G,NOR} = C_{ox}L(w_{n1} + w_{p1})$. The NOR gate's parasitic capacitance is equal to it's drain-to-bulk capacitance since we're ignoring wiring capacitance. In calculating C_{DB}, we only need to consider the two n-devices and the p-device that is connected directly to the gate output. Using the formula for C_{DB} given in the introduction, we can calculate C_{DB} for each of the three transistors and sum the resulting capacitance to arrive at the total parasitic capacitance for the NOR gate. These calculations indicate that $C_G = 0.78pF$ and $C_{DB} = 0.23pF$.

When the gate's input goes from low to high, the NOR gate's n-device turns on, discharging the energy associated with the NOR gate's own parasitic drain-to-bulk capacitance and the input capacitance associated with Inverter 1. When the gate's input goes from high to low, the gate's connected p-device turns on, charging the same capacitance. The total delay is then given by the equation for t_{PD} in the introduction using the values for C_{DB} and C_G calculated above. This delay equals 0.49 ns.

Since the n-device and p-device widths are not related by a factor of 4, we should expect somewhat skewed V_M. Using the formula given in the introduction, we calculate that $V_M = 1.56V$. In order to calculate the expected noise margins, we need to estimate the gain, A_V of the gate. This is given by:

$$A_V = -(g_{mn} + g_{mp})\frac{r_{on}r_{op}}{r_{on} + r_{op}}$$

$$A_V = -\frac{43.6w_n + 21.8w_p}{1.6w_n + 0.8w_p}$$

For the NOR gate, $A_V = -27.3$. Using the following equations to calculate V_{IL}, V_{IH}, NM_L, and NM_H, we can determine our expected thresholds to be $V_{IL} = 1.44V$ and $V_{IH} = 1.55V$ while our noise margins will be $NM_L = 1.44V$ and $NM_H = 1.44V$.

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{A_V}$$
$$V_{IH} = V_M - \frac{V_M}{A_V}$$
$$NM_L = V_{IL}$$
$$NM_H = V_{DD} - V_{IH}$$

2.2 Inverter 1

The first inverter has n and p device widths of 90 and 135 microns respectively. Consequently, it's area is simply 3038 square microns. Since it is driving Inverter 2, it sees an gate capacitance equal to the input capacitance of Inverter 2, $C_{G,1} = C_{ox}L(w_{n2} + w_{p2})$. Inverter 1 has a parasitic capacitance equal to it's drain to bulk capacitance as given in the formula for C_{DB} in the introduction. Substituting the appropriate values, we determine that the first inverter has $C_G = 2.1pF$ and $C_{DB} = 0.4pF$.

When the inverter's input transitions from low to high, the p-device shuts down while the n-device turns on. This causes the charge stored in the parasitic drain to bulk capacitance and the input capacitance of Inverter 2 to discharge through the n-device. In a similar manner, when the input goes from high to low, the p-device turns on while the n-device shuts off. This causes the parasitic capacitance of Inverter 1 and the gate capacitance of Inverter 2 to charge up through Inverter 1's p-device.

Determining the propagation delay through Inverter 1 is slightly different. Because Inverter 1 is feeding an inverter that uses a lower power supply voltage (and therefore has a lower V_M), Inverter 1 will be much slower for high to low output transitions and much faster for low to high output transitions. This is because we are measuring delay from the time Inverter 1's input reaches $V_{DD}/2$ until the time it's output reaches the V_M for the next gate. As a result, there is additional charge to dissipate during high to low output transitions while there is less charge to transfer during low to high output transitions. We account for voltage differential in the following formula, which specifies the propagation delay for Inverter 1 only:

$$t_{PD} = \frac{(C_{DB} + C_L)(2V_{DD} - V_{DDIO})L}{2W_n\mu_n C_{ox}(V_{DD} - V_{Tn})^2} + \frac{(C_{DB} + C_L)\left(\frac{V_{DDIO}}{2}\right)L}{2W_p\mu_p C_{ox}(V_{DD} + V_{Tp})^2}$$

Substituting the appropriate values, we expect Inverter 1 to have a propagation delay of 0.358 ns.

Due to the asymmetry of this gate, we expect that V_M will not be exactly equal to $V_{DD}/2$. Using the equation for V_M given in the introduction, we calculate that $V_M = 1.56V$. Using the same equations as we used for the NOR gate, we calculate that $A_V = -26.6$, $V_{IL} = 1.5V$, $V_{IH} = 1.6V$ our noise margins will be $NM_L = 1.5V$ and $NM_H = 1.36V$.

2.3 Inverter 2

Inverter 2 has n and p device widths of 204μ and 408μ respectively, indicating that Inverter 2 has a total area of 8262 square microns. Since this is the last inverter in the chain, the gate capacitance is equal to the load capacitance, $C_G = C_{Load} = 10pF$. Like the other gates, the parasitic capacitance is equal to the drain-to-bulk capacitance. Using the formula for C_{DB} given in the introduction, we can determine that $C_{DB} = 1.1pF$.

During low to high input transitions, Inverter 2's p-device turn off while it's n-device turns on, thereby discharging the load capacitor and the parasitic capacitance associated with itself. During high to low transitions, the p-device turns on while the n-device turns off, charging up the load and parasitic capacitances. The propagation delay is calculated using the standard equation given in the introduction. This yields $t_{PD} = 0.77ns$.

Since this gate is symmetric, we expect it to have a $V_M = V_{DD}/2$. Using our standard calculations, we discover that for Inverter 2, $V_M = 0.875V$, $A_V = -75.2$, while $V_{IL} = 0.86V$ and $V_{IH} = 0.89V$. Consequently, our noise margins are $NM_L = 0.86V$ and $NM_H = 0.86V$.

2.4 Summary of Hand Calculations

Gate	A_v	V_m	V_{IL}	V_{IH}	NM_L	NM_H
NOR	-27.3	1.56 V	1.44 V	1.55 V	1.44 V	1.44 V
Inverter 1	-26.6	1.56 V	1.5 V	1.6 V	1.5 V	1.36 V
Inverter 2	-75.2	0.875 V	0.86 V	0.89 V	0.86 V	0.86 V

3 Simulation Results

We conducted several simulation runs using Hspice and the sp files attached in order to verify the design. The main file is called a2c.sp and produces both a transient analysis and a DC sweep of the entire system. It also measures the total power dissipation in one cycle and the high-to-low and low-to-high pulse times. The files a2b.sp and b2c.sp produce DC sweeps of the NOR gate output and the inverter chain output as a function of the voltage at node A. The files inverter1.sp and inverter2.sp produce DC sweeps for the output of each inverter in the chain as a function of the inverter's input. Plots of the transient and DC response for the entire circuit as well as the DC sweeps described above are at the end of this report. We've also included a section of hspice output for a2c.sp indicating the total power dissipation. All these files are available on Athena in the msalib locker in the /mit/msalib/6.012/DesignProject/final/ directory.

3.1 Noise Margins

Table 2 indicates the A_v and V_m values that Hspice measured in simulation. This table also includes the calculated values for V_{IL}, V_{IH}, NM_L, and NM_H. These values were calculated using the measured A_V and V_m values and the formulas listed in the previous section.

Gate	A_V	V_m	V_{IL}	V_{IH}	NM_L	NM_H
NOR	-35.9	1.5 V	1.46 V	1.54 V	1.46 V	1.46 V
Inverter 1	-33	1.43 V	1.39 V	1.47 V	1.39 V	1.53 V
Inverter 2	-84.3	0.875 V	0.86 V	0.88 V	0.86 V	0.87 V

3.2 Spice Output File

```
* dc and transient analysis from a to c
 ******  transient analysis               tnom=  25.000 temp=  25.000
******
  tplha2c=  4.2362E-09  targ=  6.2673E-09   trig=  2.0311E-09
  tphla2c=  2.7543E-09  targ=  1.4938E-08   trig=  1.2184E-08
  tpd=  6.9906E-09
```

```
  pdiss=  3.4148E-03  from=  1.0000E-08     to=  3.0000E-08
  tphla2b=  1.0904E-09  targ=  1.3274E-08   trig=  1.2184E-08
  tplha2b=  1.0739E-09  targ=  2.3105E-08   trig=  2.2031E-08
  tplhb2c=  3.2748E-09  targ=  6.3798E-09   trig=  3.1050E-09
  tphlb2c=  1.6160E-09  targ=  1.4890E-08   trig=  1.3274E-08

        ***** job concluded
******  Star-HSPICE -- 2001.2   (20010615) 02:23:41  04/10/2002  solaris
```

3.3 Simulation file a2c.sp

```
* DC and Transient Analysis from A to C
* 6.012 Design Project

.options POST
.include "models.sp"

.param
+ wnNOR1 = 24u
+ wnNOR2 = 24u
+ wpNOR1 = 74u
+ wpNOR2 = 74u
+ wn1 = 90u
+ wp1 = 135u
+ wn2 = 204u
+ wp2 = 408u
+ ovddio = 1.75

* power supplies
vdd vdd gnd dc 3v
vddio vddio gnd dc ovddio

* circuit topology

* first inverter
Mp0 va vin vdd vdd  P15 L=1.5u W=12u AD=72p AS=72p PD=24u PS=24u
Mn0 va vin gnd gnd  N15 L=1.5u W=6u AD=36p AS=36p PD=18u PS=18u

Minvp1 vin2 vin1 vdd vdd P15 L=1.5u W=wp1 AD='6u * wp1' AS='6u * wp1' PD='12u + wp1' PS='12u +
Minvn1 vin2 vin1 gnd gnd N15 L=1.5u W=wn1 AD='6u * wn1' AS='6u * wn1' PD='12u + wn1' PS='12u +
Minvp2 vout vin2 vddio vddio P15 L=1.5u W=wp2 AD='6u * wp2' AS='6u * wp2' PD='12u + wp2' PS='1
Minvn2 vout vin2 gnd gnd N15 L=1.5u W=wn2 AD='6u * wn2' AS='6u * wn2' PD='12u + wn2' PS='12u +

Mnorp0 vnorp0 gnd vdd vdd P15 L=1.5u W=wpNOR1 AD='6u * wpNOR1' AS='6u * wpNOR1' PD='12u + wpNO
Mnorp1 vin1 va vnorp0 vdd P15 L=1.5u W=wpNOR2 AD='6u * wpNOR2' AS='6u * wpNOR2' PD='12u + wpNO

Mnorn0 vin1 va gnd gnd    N15 L=1.5u W=wnNOR1 AD='6u * wnNOR1' AS='6u * wnNOR1' PD='12u + wnNO
```

```
Mnorn1 vin1 gnd gnd gnd   N15 L=1.5u W=wnNOR2 AD='6u * wnNOR2' AS='6u * wnNOR2' PD='12u + wnNOR

CL vout gnd 10p


* analysis
vin vin gnd PULSE(0 3 0 2n 2n 8n 20n)
.tf V(vout) vin
.dc vin 0 3 .01
.tran .02n 40n

* propogation delay between va and vout for low
*  to high output transition
.measure tran tPLHa2c Trig V(va) val=1.5 TD=0 Fall=1
+ Targ V(vout) val='ovddio / 2' Rise=1

* propogation delay between va and vout for high
*  to low output transition
.measure tran tPHLa2c Trig V(va) val=1.5 TD=0 Rise=1
+ Targ V(vout) val='ovddio / 2' Fall=1

.measure tpd param='tPLHa2c + tPHLa2c'

.measure tran pdiss avg power from=10n to=30n

* propogation delay between va and vb for low
*  to high output transition
.measure tran tPHLa2b Trig V(va) val=1.5 TD=0 Rise=1
+ Targ V(vin1) val=1.5 Fall=1

* propogation delay between va and vb for high
*  to low output transition
.measure tran tPLHa2b Trig V(va) val=1.5 TD=10n Fall=1
+ Targ V(vin1) val=1.5 Rise=1

* propogation delay between vb and vout for low
*  to high output transition
.measure tran tPLHb2c Trig V(vin1) val=1.5 TD=0 Rise=1
+ Targ V(vout) val=0.925 Rise=1

* propogation delay between vb and vout for high
*  to low output transition
.measure tran tPHLb2c Trig V(vin1) val=1.5 TD=0 Fall=1
+ Targ V(vout) val=0.925 Fall=1


.end
```

3.4 Simulation file a2b.sp

```
* DC analysis from A to B
* 6.012 Design Project

.options POST
.include "models.sp"

.param
+ wnNOR1 = 24u
+ wnNOR2 = 24u
+ wpNOR1 = 74u
+ wpNOR2 = 74u
+ wn1 = 90u
+ wp1 = 135u
+ wn2 = 204u
+ wp2 = 408u
+ ovddio = 1.75

* power supplies
vdd vdd gnd dc 3v
vddio vddio gnd dc ovddio

* circuit topology

* no first inverter!
Minvp1 vin2 vin1 vdd vdd P15 L=1.5u W=wp1 AD='6u * wp1' AS='6u * wp1' PD='12u + wp1' PS='12u +
Minvn1 vin2 vin1 gnd gnd N15 L=1.5u W=wn1 AD='6u * wn1' AS='6u * wn1' PD='12u + wn1' PS='12u +
Minvp2 vout vin2 vddio vddio P15 L=1.5u W=wp2 AD='6u * wp2' AS='6u * wp2' PD='12u + wp2' PS='1
Minvn2 vout vin2 gnd gnd N15 L=1.5u W=wn2 AD='6u * wn2' AS='6u * wn2' PD='12u + wn2' PS='12u +

Mnorp0 vnorp0 gnd vdd vdd P15 L=1.5u W=wpNOR1 AD='6u * wpNOR1' AS='6u * wpNOR1' PD='12u + wpNO
Mnorp1 vin1 va vnorp0 vdd P15 L=1.5u W=wpNOR2 AD='6u * wpNOR2' AS='6u * wpNOR2' PD='12u + wpNO

Mnorn0 vin1 va gnd gnd    N15 L=1.5u W=wnNOR1 AD='6u * wnNOR1' AS='6u * wnNOR1' PD='12u + wnNO
Mnorn1 vin1 gnd gnd gnd   N15 L=1.5u W=wnNOR2 AD='6u * wnNOR2' AS='6u * wnNOR2' PD='12u + wnNO

CL vout gnd 10p


* analysis
va va gnd PULSE(0 3 0 2n 2n 8n 20n)
.tf V(vin1) va
```

```
.dc va 0 3 .01


.end
```

3.5 Simulation file b2c.sp

```
* DC Analysis from B to C
* 6.012 Design Project

.options POST
.include "models.sp"

.param
+ wnNOR1 = 24u
+ wnNOR2 = 24u
+ wpNOR1 = 74u
+ wpNOR2 = 74u
+ wn1 = 90u
+ wp1 = 135u
+ wn2 = 204u
+ wp2 = 408u
+ ovddio = 1.75

* power supplies
vdd vdd gnd dc 3v
vddio vddio gnd dc ovddio

* circuit topology

* no first inverter or NOR gate!
Minvp1 vin2 vin1 vdd vdd P15 L=1.5u W=wp1 AD='6u * wp1' AS='6u * wp1' PD='12u + wp1' PS='12u +
Minvn1 vin2 vin1 gnd gnd N15 L=1.5u W=wn1 AD='6u * wn1' AS='6u * wn1' PD='12u + wn1' PS='12u +
Minvp2 vout vin2 vddio vddio P15 L=1.5u W=wp2 AD='6u * wp2' AS='6u * wp2' PD='12u + wp2' PS='1
Minvn2 vout vin2 gnd gnd N15 L=1.5u W=wn2 AD='6u * wn2' AS='6u * wn2' PD='12u + wn2' PS='12u +

CL vout gnd 10p

* analysis
vin1 vin1 gnd PULSE(0 3 0 2n 2n 8n 20n)
.tf V(vout) vin1
.dc vin1 0 3 .01
```

```
.end
```

3.6 Simulation file inverter1.sp

```
* Inverter 1 Analysis
* 6.012 Design Project

.options POST
.include "models.sp"

.param
+ wnNOR1 = 24u
+ wnNOR2 = 24u
+ wpNOR1 = 74u
+ wpNOR2 = 74u
+ wn1 = 90u
+ wp1 = 135u
+ wn2 = 204u
+ wp2 = 408u
+ ovddio = 1.75

* power supplies
vdd vdd gnd dc 3v
vddio vddio gnd dc ovddio

* circuit topology

* no first inverter or NOR gate!
Minvp1 vin2 vin1 vdd vdd P15 L=1.5u W=wp1 AD='6u * wp1' AS='6u * wp1' PD='12u + wp1' PS='12u +
Minvn1 vin2 vin1 gnd gnd N15 L=1.5u W=wn1 AD='6u * wn1' AS='6u * wn1' PD='12u + wn1' PS='12u +
Minvp2 vout vin2 vddio vddio P15 L=1.5u W=wp2 AD='6u * wp2' AS='6u * wp2' PD='12u + wp2' PS='1
Minvn2 vout vin2 gnd gnd N15 L=1.5u W=wn2 AD='6u * wn2' AS='6u * wn2' PD='12u + wn2' PS='12u +

CL vout gnd 10p

* analysis
vin1 vin1 gnd PULSE(0 3 0 2n 2n 8n 20n)
.tf V(vin2) vin1
.dc vin1 0 3 .01


.end
```

3.7 Simulation file inverter2.sp

```
* Inverter 2 Analysis
* 6.012 Design Project

.options POST
.include "models.sp"

.param
+ wnNOR1 = 24u
+ wnNOR2 = 24u
+ wpNOR1 = 74u
+ wpNOR2 = 74u
+ wn1 = 90u
+ wp1 = 135u
+ wn2 = 204u
+ wp2 = 408u
+ ovddio = 1.75

* power supplies
vdd vdd gnd dc 3v
vddio vddio gnd dc ovddio

* circuit topology

* no first inverter or NOR gate or first inverter in chain!
Minvp2 vout vin2 vddio vddio P15 L=1.5u W=wp2 AD='6u * wp2' AS='6u * wp2' PD='12u + wp2' PS='1
Minvn2 vout vin2 gnd gnd N15 L=1.5u W=wn2 AD='6u * wn2' AS='6u * wn2' PD='12u + wn2' PS='12u +

CL vout gnd 10p

* analysis
vin2 vin2 gnd PULSE(0 3 0 2n 2n 8n 20n)
.tf V(vout) vin2
.dc vin2 0 3 .01


.end
```